AD-A117 459 NATIONAL MATERIALS ADVISORY BOARD (NAS-NAE) WASHINGTON DC F/G 9/5
AN ASSESSMENT OF THE IMPACT OF THE DEPARTMENT OF DEFENSE VERY-H--ETC(U)
JAN 82 J ST. CLAIR, N G EINSPRUCH, W G HOWARD N00039-80-C-0125
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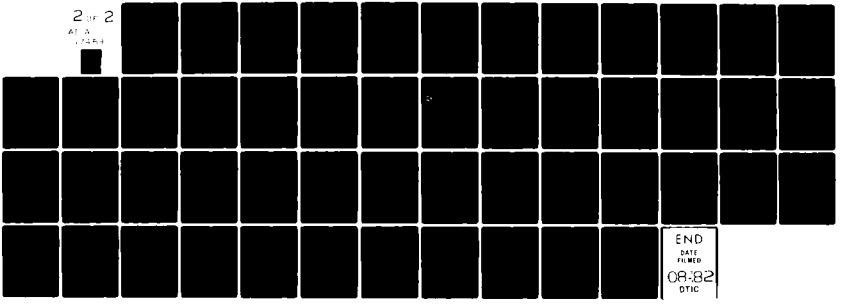

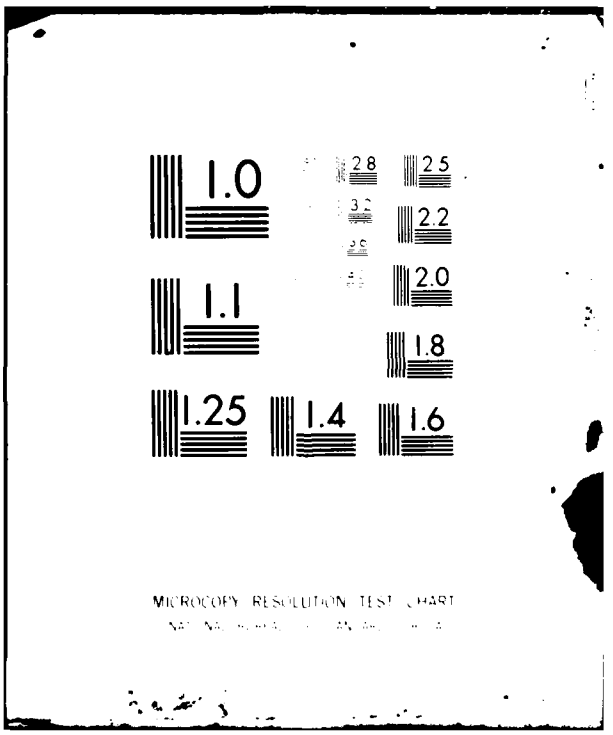
1.0
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MICROCOPY RESOLUTION TEST CHART

Electrical uniformity is important to those circuits that are influenced by substrate resistivity. Effect of wafer-to-wafer variations can be reduced by ion implantation of critical features. However, this adds processing steps and cannot compensate for variations within a wafer. For larger wafer sizes (4 to 6 in.) both topographic and electrical uniformity need to be improved.

Sensitivity to radiation also is related to materials. It has been reported that chromium impurities in sapphire affect the radiation hardness of SOS circuits. The presence of metallic ions in silicon leads to mobile (and immobile) ionic charges in silicon dioxide. Heavy-metal atoms in the substrate provide recombination centers that shorten carrier lifetime and attenuate the effects of ionizing radiation in the conducting substrates. Carriers caused by ionizing radiation otherwise might be collected at the surface and cause an upset. Heavy-metal atoms adversely affect the electrical properties of the silicon.

The impact of new materials on VHSIC reliability should be considered. For example, polyimide is being considered as a conformal dielectric coating between multilevel metal interconnect layers. Polyimide films have rounded edges and very low dielectric constant. As a consequence, polyimide improves the step coverage of the second layer of metal where it crosses the first layer metal and also reduces the crosstalk between interconnect layers. Furthermore, polyimide acts as an absorbing shield to alpha-particle radiation. However, since it is an organic compound there is some concern about its long-term stability. It is hygroscopic and any water vapor reaching the film would expand it. Long-term reliability studies will be needed.

Inorganic chemical processes are governed by diffusion phenomena. Therefore, they tend to obey the Arrhenius failure model and this permits accelerated life testing of chips at elevated temperatures. For chips that contain materials with low-temperature phase changes, the Arrhenius model may be invalid. Accelerated life-test data may be either too optimistic or too pessimistic. A thorough understanding of failure mechanisms in the latter materials is needed.

Processing Technology and Limitations

Probably the most crucial and yet least understood step in the manufacture of ICs is slice processing. At this stage the design, as reflected in a set of photomasks or a program for electron-beam direct slice writing, comes together with the materials in a single critical pathway consisting of highly interdependent steps. Although great strides are being made in scientific understanding of the processes that constitute slice fabrication, it remains largely an art in that many process parameters are empirically derived, and process steps are included because they are found to solve particular problems for unknown reasons. This situation probably will

continue into the submicrometer regime because new materials and processes are being introduced in order to solve particular problems at a rate that is inconsistent with their assimilation in a totally rational manner.

Generally speaking, the processing problems addressed here are common to all of VLSI, although their severity depends on the particular device and process technologies employed. In addition, some manufacturers have made more progress in solving them than others. These problems affect both the phase-I and phase-II VHSIC efforts, but their impact on each is different. At the 1.25-μm line-widths of phase I, they generally fall into the class of annoyances that will tend to limit yield and impose stringent design constraints, but that are not true barriers to achievement of phase-I goals. However, many of them become essentially insurmountable barriers to achieve phase-II goals using current process technology. In these cases, new process development is required as discussed below to solve the problems. These development efforts are, or will be, included in all three phases of the program. Even greater effort to solve them will be applied outside the VHSIC program because of the commercial importance of VLSI, and this should have a salutary effect on the program.

It is difficult to separate processing from device technology because of the intricate coupling of device and structure considerations with fabrication. Indeed, the necessity of this coupling has become compelling in current VLSI-VHSIC technology development. The limitations and challenges in processing become particularly acute as minimum geometries shrink below 1 micrometer, and these limitations all relate to five central device technology issues whose resolution will determine the extent to which solid-state devices may be scaled to provide increasingly complex ICs vis a vis the limits dictated by thermodynamics, quantum mechanics, and materials properties. The issues which have been discussed in part earlier, are:

1. Improvement of intrinsic device gain while avoiding adverse effects on yield and reliability.

2. Reduction of parasitic resistances and capacitances.

3. Increase in interconnectivity--the universal communication problem.

4. Avoidance of noise margin, "soft error" and radiation-resistance problems.

5. Control of pattern definition in three dimensions, defect density, and solid-state reactions involving thin material layers.

The ensuing discussion will address the structure-process and manufacturing considerations that relate to the above five issues.

STRUCTURE-PROCESS

Isolation. The Local Oxidation of Silicon (LOCOS) isolation approach is in wide use today and has permitted the rapid shrinking of circuit geometries as witnessed in the 1970s. However, inherent in this approach are oxide and channel stop encroachments into the active device region which result in a minimum, nonscalable transition region between active device and device isolation of the order of 1 to 2 micrometers. This nonscalability leads to excessive dedication of silicon "real estate" for isolation as other geometries are scaled. In addition, this isolation approach is known to cause stress- and defect-induced leakage current in the transition region that is more harmful at higher densities due to its relatively larger effect on smaller capacitances and signal currents. A low capacitance, planar isolation approach is required which has a minimum transition region on the order of < 0.1 micrometers.

Gate Insulator. Successful scaling of the MOSFET as regards improved gain requires increased gate insulator capacitance. Although a saturation point finally is reached due to the inversion layer capacitance that is in series with the gate capacitance, this point is not reached until the gate oxide thickness is reduced to 5 to 7nm. Today's gate oxides range 40 to 80 nm in thickness, so that the gate capacitance can be increased by decreasing the thickness of the conventional SiO_2. However, it becomes increasingly difficult to realize such thin insulators that also exhibit high yield and reliability, especially at VLSI levels of integration. Alternatively, a thicker, high dielectric constant insulator may be considered as a replacement for SiO_2. However, it must have interfacial electronic properties equal to that of the SiO_2 silicon interface in order to be acceptable.

Parasitic Resistance. The parasitic resistance issue has become of paramount importance because the point is being reached in the scaling of devices at which the expected improvements in circuits due to improved intrinsic device performance cannot be realized without substantial reduction in the series parasitic resistance. These resistances include the gate electrode and interconnect that today is doped polysilicon, source-drain resistance, contact resistance (between source-drain and metallization), interconnects, and substrate. Conventional circuits use doped polysilicon whose lower resistance limit is $\approx$ 20 ohms/square. Silicide-polysilicon sandwich layers offer improvements down to 1 ohm/square. However, even lower, metallic-like resistance is desired which is also compatible with the gate insulator from the reliability point of view.

With regards to the source-drain resistance, successful device scaling dictates very shallow souce-drain junctions. However, with the conventional ion-implanted source-drain approach, the resistance increases precipitously (x_j^{-n}, $n = 5$-10) as the junction depth x_j is decreased below 0.25 micrometers, so that the device gain is degraded seriously by excessive source-drain series resistance. Totally new approachs are required to overcome this limitation. In addition, as geometries are scaled, contact

openings between metallization and the silicon likewise must scale with a resulting increase in contact resistance. Even with the lowest contact resistance reported to date ($\sim 10^{-7}$ ohm-cm^2) a series resistance of 160 ohms results from a single contact when the contact opening decreases to 0.25 0.25 micrometers^2. This is unacceptably high if high-performance submicron circuits are desired.

Parasitic Capacitance. The point was made above that device scaling was reaching a stage at which further expected improvements in device perfomance would be limited unless reductions in both parasitic resistance and capacitance could be realized. Analysis verified by experiment has shown that maximum benefit in capacitance reduction can be achieved through the use of minimum dielectric constant insulators with thicknesses between levels of interconnects equal to the linewidths and spacings of the interconnects themselves. This guideline dictates the use of structures (lines, contact openings, etc.) having very large aspect ratios (i.e., planar dimensions equal to vertical dimensions). These are much more difficult to fabricate with control. Moreover, since chip size does not decrease as device geometries decrease, and since it is extremely difficult to proportionately decrease the mean communication distance between devices and circuit elements, this parasitic capacitance does not decrease. Here, revolutionary approaches spanning the spectrum of architecture, circuit design, and device technology are required.

Interconnectivity. The interconnectivity issue is typical of the universal problem of providing for adequate low-noise, high-speed communication links (metal lines) between increasing numbers of entities (device and circuit elements). The number of levels of metallization can be increased; however, the difficulties in realizing metal coverage of topographically varying surfaces, high yield, high aspect-ratio contact patterning, and high-resolution metal patterning increase exponentially with the number of metal levels.

Particle Induced Upset and Radiation Resistance. It is well known that parts-per-million (ppm) traces of naturally occurring radioactive elements can result in "soft errors" due to high energy particle (1 to 5 MeV alpha particle) emission into the bulk silicon near the active circuits. Because of this phenomenon, the use of materials in the actual device fabrication is restricted to only those materials that do not possess radioactive isotopes or impurities having alpha particle emissions. As capacitances, currents, and signal sizes further decrease with scaling materials having other, lower energy decay events from radioactive isotopes or impurities also must be avoided. Cosmic ray-induced particles also represent a major limitation at smaller geometries, and their shielding is literally impossible. Thus, new fabrication approaches based on new structures, starting substrates, and materials will be necessary.

At present it is known that certain steps in IC fabrication will degrade the radiation hardness of circuits, which is a property of special importance to military devices. Examples are the use of hydgrgen, high temperatures, and

dry etching processes that include high energy radiation after the gate insulator has been formed in the IC processing. However, avoidance of the use of these processing steps seriously compromises the ability to fabricate highly reliable ICs with close control of physical and electrical parameters.

Manufacturing

Defect Density. The reduction of defect density has consumed, and will continue to consume major resources in IC manufacturing. The science of process defects (chemical contamination, dust, lithography, etching, film depositions, thermal, etc.) is not well developed at this time with limited understanding of the causes and cures of process defects. In addition, development of higher density ICs continues to expose previously incipient defects so that large reductions (comparable in scale to linewidth reductions) in defect densities have not been possible to date. However, smaller circuit geometries and larger levels of integration as well as improved reliability will require significant decreases in the levels of defects.

Pattern Definition Control. The fabrication of ICs today requires pattern definition control ranging around ± 0.5 micrometers for a 5-micrometer linewidth, or $\pm$ 10 percent. If the same degree of control is to be maintained when geometries approach 0.5 micrometer, then a routine pattern definition capability (lithography plus etching) of $\pm$ .05 micrometer, or $\pm$ 500 Å must be available. This extrapolates to $\pm$ 100 Å for successful exploitation of 1000 Å geometries. Clearly, major challenges exist as regards the achievement of this required control for large chips containing millions of devices with many meters of interconnects. In addition, the need for and the trend to larger aspect ratio features in films aggravates the pattern definition control by requiring very high anisotropy and selectivity in the etching of such films. Unfortunately, high aspect ratios cannot be avoided in interconnects and contact openings because of the mandatory need for very low interconnect resistance and low capacitance. Finally, the achievement of higher resolution appears to require higher energy forms of dry etching (ion milling, etc.). It is known that in some cases circuit reliability may be compromised due to gate insulator damage caused by higher energy etching.

Parameter Control. Tight control of process parameters is necessary in IC fabrication in order to provide maximum noise margin, and, hence, maximum operating temperature range and tolerance to supply voltage variations. This is true because electric parameter control depends strongly on the control of process parameters such as linewidth, impurity doping profiles, film thicknesses (e.g., gate insulator), series and contact resistance, and threshold voltage. As device geometries continue to decrease, much tighter control is required. This is because supply voltages also must decrease, and if electric parameter variations are to remain a constant percentage of the supply voltage, then their absolute control must improve. Just as important is the limitation arising from the fact that some electrical parameters do not

scale with decreased device size and voltage. Examples are subthreshold leakage and the temperature variation of the threshold voltage. As a result, the total parameter variation remains constant and represents a larger fraction of the supply voltage as the supply voltage is decreased. This makes it increasingly difficult to maintain the same operating temperature range and radiation hardness in circuits, and it places even greater pressure on process parameter control.

Process Complexity. In the past decade there has been a trend towards increased process complexity in IC fabrication. This is a result of continuous competitive pressure for improved circuit performance and greater functional capability as well as increased sophistication in silicon technology. The increased functional complexity, of course, has been realized primarily by decreasing geometries and structural cleverness, and it is these approaches that have required greater complexity in the process. However, the increased process complexity typically results in greater defect densities and, consequently, lower yields, which is totally counter to fabrication requirements at very high levels of integration based on ever-decreasing goemetries.

MANUFACTURING AND TEST EQUIPMENT

Through the courtesy of Dr. Larry Hansen, Varian, the committee was provided with an excellent review of the status of equipment technology and equipment manufacturing and a suggestion that further equipment development be directly funded as an integral part of the VHSIC program (Appendix H). The VHSIC program management office has chosen to fund selected portions of equipment development but to do this through existing prime contractors. The committee believes that the equipment needs of the VHSIC program are being recognized and addressed, and that the choice of funding mechanism is a matter outside of the committee's purview.

Optical Lithographic Equipment

New state-of-the-art systems are capable of 1.25-micrometer feature size using mercury 3000-Å sources. Current production systems can process 15 wafer levels per hour on 4-inch wafers. There is a trade-off between alignment time and registration accuracy. For that reason, self-aligning processes that are less sensitive to registration will receive more emphasis.

One potential DoD problem in optical lithography is that all lenses for precision measurements are made overseas in France, Germany, and Japan. Furthermore, there is talk that the most advanced photolithography system is made by Censors, Inc., a company based in Liechtenstein. State-of-the-art machines will be available to Eastern Bloc countries.

The VHSIC program could have a negative impact on the supply of photolithography equipment by increasing demand over the next two years. After that, the effect should be negligible. A summary of some equipment cost and availability is given in Table 15.

Table 15. Cost and Availability of Photolithography Equipment.

EQUIPMENT	COST ($K)	DELIVERY (MOS)
Contact-proximity alignment	40/80	6
Projection alignment	250	12
DSW	600	12
Resist processing	200	12
Etching	100	9
Inspection	60	9
Mask Making		
Pattern generator-optical	500	12
Mask inspection (Comparator, etc)	400	12

Electron Beam and X-Ray Lithographic Equipment

E-beam lithography is becoming main stream for mask-making for more complex ICs. Experiments with direct write electron beam lithography are currently under way and are receiving significant funding under VHSIC phase III. In appendix H some additional insight into this activity is described. Because of the limited availability and long delivery time of the equipment, this is an area in which the VHSIC program is likely to affect commercial IC activities, but it is believed that this effect will be slight. E-beam machines currently cost on the order of $2 million with delivery times of 12 to 18 months. Direct step E-beam lithography is the subject of major development by the equipment manufacturers.

X-ray lithography is in an earlier stage of development but it could eventually be more cost-effective than e-beam lithography. The first production x-ray lithographic equipment is currently being announded. The fabrication of defect-free masks is probably the most significant barrier to be overcome in order to make this technology useful for VHSIC.

Other Processing Equipment

The semiconductor equipment industry is healthy and the manufacturers of thei equipment are able to supply the IC industry's needs (see Appendix H). Routine equipment such as diffusion ion implantation, metalization, and wafer handling should not be a problem. Dry etching will require additional work as will equipment to provide improved silicon.

Test Equipment

Commercial suppliers are pushing ahead in the general direction of VHSIC requirements. However, the projected pin limitations of 120 pins may be marginal as are the projected speed limitations of 20 to 30 MHz. The most advanced tester in development is believed to be in Japan--384 pins at 100-MHz speeds.

Availability of equipment, does not appear to be a problem. The next generation of testers was scheduled for introduction in 1981, and the manufacturers claim that they are not production-limited, as indicated in Table 16.

The cost of test equipment however, is a problem. These machines are expected to be in the $1 to $3 million plus price range when fully configured. This is an order of magnitude increase since 1976.

The VHSIC program is expected to have no negative impact on the test-equipment industry

Technology Insertion

The advanced ICs to be delivered under the VHSIC program are intended to provide the DoD with significant potential capabilities in the signal-processing area. These capabilities will be realized only when the parts are incorporated into military electronics systems in the inventory.

The development and procurement cycle for military equipment has become long and complex. Because of the critical need for the equipment, a number of reviews and check points have been inserted into the procedure. Although these reviews may well help to insure the overall success of the program, they introduce a strong measure of conservatism that is difficult for any new technology to overcome. This will be particularly true in the case of VHSIC parts.

Table 16. VHSIC Testing Systems (a Preliminary Summary)

Manufacturer/ Model	Pins/ Channel	OP. Freq. (AG./SGL.CH.)	Stations/ System	Delivery	Typical Delivered Price	REMARKS
Century Series 20 Fairchild, (U.S.)	120	20 MHz	2+	5 mo.	$800K	Available 50 MHz in 1-1/2 Yr.
Series 7900 System Accutest, (U.S.)	64 Dr. 64 RVR	25 MHz 50 MHz	2+	6-9 mo.	$450K	100 MHz and increased I/O C is being studied; true parallel test
T3300 Series Riken Takeda (Japan)	384	100 MHz 100 MHz	2+	12 mo.+	$3.5M	384-pin split test under development
Q2-60 Series	40/Head (160)	20 MHz 20 MHz	4	3-4 mo.	$336K	Only 10 MHz for 4-head true parallel test
J325 System Teradyne, (U.S.)	84	20 MHz 20 MHz	2+	4 mo.	$130K	50 MHz for memory device test
S-3270 System Tektronics	64	20 MHz	2	5 mo.	$680K	Driver and receiver per pin no anticipated operator frequency increase within a year.

In the past some major procurements have required the concurrent development of the components with the systems. Although procurement of strategic systems by this technique has been quite successful, the technique has not been commonly used for smaller systems. If the procurement cycle is to be appreciably shortened, this practice must become .the norm for systems with VHSIC parts. It is hoped that a portion of the proposed phase-III effort can be used to consider advanced procurement practices that will substantially reduce these very long lead times.

Two different approaches are being pursued by the phase-I VHSIC contractor. One group is pursuing an approach in which a basic family of standard parts would be modified for specific applications by software techniques or by minor physical modifications (gate arrays). The second approach is one in which basic building blocks would be assembled as photomasks and used to produce unique parts for each application.

The standard parts approach will present fewer problems in technology insertion. These parts will fit into the military parts qualification procedure with little difficulty. Parts designed for specific systems will present several new but solvable problems. Procedures will be required for the acceptance of design rules, as well as those for the monitoring of a given production process. Although some consideration has been given to both problems, substantial effort will be required to develop viable quality assurance technicians for devices of this type.

Although the VHSIC program has been structured to assure the availability of a second source for the parts to be delivered, acceptance of the program would be enhanced if some degree of standardization were encouraged among the contractors. Even though the product functions will differ, agreement on supply voltage and packaging among the contractors would speed their adoption into real systems.

In the past, semiconductor parts developed under military contract have been usually offered for sale by semiconductor houses and purchased by the equipment makers as needed. The degree of vertical integration provided by the VHSIC program should minimize delays in acceptance of these new parts, but it will not eliminate them.

It is the understanding of the committee that specific military systems will be designated for VHSIC applications in the near future and that funds will be provided for their procurement. Until this has been done, and the increased capability and projected costs of the new equipment determined, the full impact of VHSIC on the DoD cannot be assessed.

CONCLUSIONS

No fundamental physical limits are forseen that threaten the attainment of the VHSIC technical goals.

Successful realization of VHSIC component capability is strongly dependent on design automation. All phases of VHSIC chip production are affected. Although simulation capability generally is adequate, some work remains to be done in layout automation and design-rule checking, and substantial progress must be made in layout verification. Test generation is a critical unsolved problem.

Emphasis has been properly placed on Design, Architecture, Software and Test (DAST) by the VHSIC program for it is essential to achieve VHSIC objectives. Experience has shown that university and industrial efforts are complementary in the development of computer aids to design.

The VHSIC program is to be commended for supporting research on code generation and architecture for signal processors. The great importance of these issues calls for additional effort by the DoD Research and Development programs in these fields and in other aspects of software related to VHSIC.

Some new developments in IC materials clearly will be required, but there is no reason to believe that this will present a major problem to the VHSIC program or have a major impact on the industry.

Although a degree of commonality in processing is anticipated between commercial VLSI and VHSIC devices, the unique environmental requirements of the military services will call for a substantial effort in process development to assure radiation-hardness of the parts against nuclear radiation.

The process equipment needs of phase I can be met by commercial offerings now available in the IC industry. Phase II of the program may require additional equipment development, particularly in the lithography area. These requirements are not likely to produce a major perturbation for the equipment manufacturers or the commercial IC industry.

Although it is the committee's opinion that successful completion of the VHSIC program will have a significant effect on maintaining the United States lead in military applications of ICs, the full impact of the program on DoD systems cannot be fully assessed until the designation of equipment for specific military systems is completed and funding for their procurement has been provided.

APPENDIX A

HOUSE ARMED SERVICES COMMITTEE REPORT ON DEPARTMENT OF DEFENSE AUTHORIZATION ACT, FISCAL YEAR 1980

(HOUSE REPORT 96-166, May 15, 1979, pp. 102-103).

Very High Speed Integrated Circuits

Committee Recommendation

The committee recommends against the entire authorization requests for Very High Speed Integrated Circuits development programs in the following amounts: $12.0 million for the Army; $10.43 million for the Navy; and $8.0 million for the Air Force.

Basis for Committee Action

These requests are for the initiation of an estimated $200 million government investment to support industrial development of new electronic devices for the next generation of military systems. The justification for requesting such government investment is the fact that: "The current trend in the semiconductor industry is towards the development of general purpose integrated circuits to be used in the commercial market. This industry is not sufficiently oriented towards qualifying integrated circuits for military specifications. . . ."

The recommendation for these programs is intended as a deferral and not as a termination. The committee supports the need for such potentially high payoff research and development programs. However, in this instance, there is a policy conflict which should be resolved before authorization and appropriation of funding. The issue of concern is how will a mechanism be established for transferring the know how gained from government supported research programs to other companies in the semiconductor industry so that future military system procurement contracts can be awarded in as competitive a market structure as possible. Currently, the Defense Department intends on using established procedures for assuring that government funded technology developments can be transferred to other companies. However, questions which these procedures have not adequately addressed include: how will future agreements be arrived at to identify acceptable companies for receiving information developed under such contracts; how much background knowledge relied upon by the developing contractors will be released to the government for transfer to other companies; and will the government or the developing contractor be responsible for transferring this knowledge? Until these questions are resolved, any commitment by the government could result in a small number of industry participants, which receive early government support, becoming the major sources of critical electronic devices for our future military systems. The committee, also, does not support authorizing several program elements for this effort. A single program should be established.

APPENDIX B

VHSIC AUTHORIZATION REQUEST APPROVAL

CONFERENCE REPORT ON DEPARTMENT OF DEFENSE AUTHORIZATION ACT, FISCAL YEAR 1980

(HOUSE REPORT 96-546, October 23, 1979, pp. 41-42)

Very high-speed integrated circuits

The Senate bill authorized $12.0 million for the Army, $10.43 million for the Navy, and $8.0 million for the Air Force to begin development of very high-speed integrated circuits. The House amendment provided no authorization for this work. *The conferees agreed to* authorize the full amount requested.

In approving the authorization for $30.43 million, the conferees established a new program line in the Air Force titled Very High-Speed Integrated Circuits. Management of this tri-service program, including funding control, is to be executed by the Under Secretary of Defense for Research and Engineering.

The conferees concurred in the concerns of the House and approved authorization for this program with the following understanding:

The export of the technology developed in this program would be controlled where applicable by the International Traffic in Arms Regulations until the state-of-the-art for such technology progresses to the point where national security permits its transfer to other controls for export.

The contracts awarded for this program must include the clauses contained in amendment number 0003 dated September 24, 1979, to the Request for Proposals issued for this program on June 22, 1979. These clauses provide the Government the option of having licenses granted so that the technology developed under this program can be used in practice by the Department of Defense and its contractors as needed for future programs.

APPENDIX C

QUESTIONNAIRE
ON IMPACT OF VHSIC PROGRAM
ON IC AND RELATED INDUSTRIES

DEPARTMENT OF THE NAVY
Office of the Assistant Secretary
(Research, Engineering and Systems)
Washington, DC 20350

8 Aug. 1980

Dear Dr._____:

The National Materials Advisory Board (NMAB) has been asked by the Department of Defense (OUSDR&E) to study the technical and economic impacts of the DoD's development program for Very-High-Speed Integrated Circuits (VHSIC). The study will attempt to assess the effects of the VHSIC program on the integrated circuit industry and related industries.

An important aspect of this study is the impact of the VHSIC program on private industrial R&D. I am the chairman of the subcommittee which is responsible for this part of the study. Your company is an important member of the integrated circuit industry, and I would very much appreciate your input. My initial report is due on the 15th of September. This constraint does not permit me to speak to each of you individually, so I hope to involve you by seeking your cooperation in answering the questions contained in the enclosure. If you have any questions, I can be reached at (202) 695-1444 or you may contact Mr. C. E. Holland, Jr., at (714) 225-6860. Please address your responses to:

Mr. C. E. Holland, Jr.
Naval Ocean Systems Center
Code 9205
San Diego, CA 92152

I know your input will make an important contribution to the NMAB study. I appreciate your cooperation in this study and would like very much to receive your response by 20 August.

Very truly yours,

D. F. Barbe
Subcommittee Chairman

Enclosure

THE RELATIONSHIP OF THE THRUST AND MAGNITUDE OF THE VHSIC PROGRAM TO PRIVATE INDUSTRY EFFORT

The VHSIC program will invest approximately 200M dollars over the next six years, in integrated circuit R&D and signal processing applications. Perhaps the most effective way to define the thrust and magnitude of VHSIC is to identify the major areas of technical activity and the planned level of expenditure.

THRUST	MAGNITUDE ($ IN MILLIONS)
Lithography & Processing	35
Design, Architecture, Software and Test	70
Pilot Line Development	52
Systems Design	20
Systems Fabrication & Demonstration	32

The subcommittee which I chair is trying to determine if private sector R&D is or is not likely to be affected either in magnitude or direction by the VHSIC program. Using the above data, please discuss the impact, if any, the VHSIC program will have on your independent research and exploratory development (IR/IED) program. If company funded R&D is not included in the IR/IED, please discuss it also.

ENCLOSURE

The organizations that responded to the inquiry were:

Government Agencies

- Army
- Navy
- Air Force
- DARPA
- NASA
- NSF
- NBS

Military Systems Manufacturers

- Raytheon
- Hughes Aircraft Co.
- Hughes Aircraft Co. (Research Labs)
- Honeywell
- Westinghouse Electric Corp.
- Boeing International
- Rockwell International

Merchant Semiconductor Firms

- Fairchild Camera & Instrument
- National Semiconductor
- RCA
- Motorola
- Bell Labs (listed in this category for convenience)

Semiconductor Equipment Firms

- Perkin-Elmer Corp.
- Varian/Extrion

Universities/Research Institutes

- Cornell University
- University of Arizona
- Rensselaer Polytechnic Institute
- California Institute of Technology
- Research Triangle Institute
- The University of Texas at San Antonio
- University of Illinois

APPENDIX D

DOD GUIDELINES FOR APPLICATION OF THE ITARs
OFFICE OF THE UNDER SECRETARY OF DEFENSE

Washington, D.C. 20301

December 12, 1980

MEMORANDUM FOR VHSIC PROGRAM DIRECTORS

SUBJECT: Export Control Interim Guidance for VHSIC Contract Monitors and Contract Officer Technical Representatives

The application of export controls (International Traffic in Arms Regulation [ITAR] and Export Administration Regulations [EAR]) contemplated for the VHSIC program was discussed at the 4 December seminar. This memorandum provides interim guidance for COTRs and Contract Monitors with respect to VHSIC contracts.

Devices (Circuits)

Devices developed under the program for military applications (not experimental devices for process development) are subject to ITAR control. All other devices are subject to the Commodity Controls of the EAR. Export applications are to be made by the contractor to State (ITAR) or Commerce (EAR). COTRs and Contract Monitors have no direct responsibility for such proposed exports unless requested to participate in evaluations of military applicability or technical content by the Program Office. COTRs and Contract Monitors are responsible for alerting contractors to the applicability of controls and for avoiding approval of actions limited by the controls. As an example, the temporary export of controlled items for display in foreign countries at trade shows, etc., is not permitted if the controlled item would not normally be licensed for export. COTRs and Contract Monitors should not appear to give consent to such participation in trade shows, etc., but should refer the contractor to the appropriate Department (State, Commerce).

Manufacturing and Process Equipment

Manufacturing equipment is subject to EAR controls with the exception of newly developed equipment not described in the EAR. Such equipment will be controlled under the ITAR until the EAR is revised to accommodate it. Guidance for COTRs and Contract Monitors is the same as for Devices.

Technical Data

Technical Data may be subject to control by the ITAR or the EAR. Controlled technical data does not include information normally considered to be basic science, such as information related to materials properties, physical and chemical reactions, fundamental physical limitations, stress analysis, statistical inference, device physics and other such products of basic research. Examples of such information would be: analyses of properties of materials, including transport phenomena, contact metallurgy, etc; analyses of physical reaction, such as bulk versus surface properties, electronic and chemical aspects of interfaces, etc.; research on tunneling, electromigration, etching kinetics, etc; studies of the interiors of composites; stess and defect analyses; modeling of electronic and magnetic characteristics; and software design concepts of a general nature.

The distinction that is being made is between basic science, the results of basic research and process or utilization technology. The former are not subject to controls while the latter are. COTRs and Contract Monitors are expected, during pre-publication review, to determine if the subject matter falls into the category of basic research or into the category of process or utilization technology. The first can be released through normal channels. The second should be reviewed with the contractor to see if modifications can be made to permit open publication. If it cannot be so modified, and publication is still desirable, the document should be clearly marked:

> "This document contains technical data subject to control under the International Traffic in Arms Regulations. Disclosure to foreign nationals, except under certain restricted conditions, is not authorized. Contact the office below prior to any such disclosure."

and the office address and telephone number of the COTR or Contract Monitor should appear beneath the marking. Technical data under such control cannot be presented at open symposia or meetings, nor can such reports be cleared for distribution through sources such as NTIS.

Particularly in the early stages of the program it may be difficult for COTRs and Contract Monitors to make a clear determination if the subject material belongs in the uncontrolled, basic research category or is controlled process or utilization technology. In case of doubt, or of substantial disagreement by the contractor, the proposed publication should be forwarded to the Program Office for review and decision. This process will help to refine the guidelines and to ensure uniform application of controls throughout the program.

In case of basic research supported by the VHSIC program, although such research and its results are not generally controlled, it is the preference of the Program Office that only U.S. citizens participate. Where this preference cannot be accommodated, the contractor should be directed to the Program Office for resolution. This does not apply to contractors operating under a technical assistance agreement approved by the Department of State.

Larry W. Sumney
Director, VHSIC

APPENDIX E

LETTER SOLICITING EXPERT OPINION ON MANPOWER ISSUES
AND LIST OF RESPONDENTS

University of Miami
Coral Gables, Florida 33124
SCHOOL OF ENGINEERING AND ARCHITECTURE
P.O. Box 248294 (305) 284-2404

August 12, 1980

Mr. Alfred J. Stein
Vice Presider nd Assistant General Manager
Motorola Inc.
Semiconductor Group
P.O. Box 2953
Phoenix, Arizona 85062

Dear Al:

The National Research Council (National Academy of Sciences/National Academy of Engineering) recently established a panel charged with "Assessment of the Impact of the DoD Very High Speed Integrated Circuit (VHSIC) Program."

As a member of the panel, I was asked to research the issue of the impact of the VHSIC program on scientific and engineering manpower. To accomplish this end, I am writing to you and to a very limited number of others in industry and academia who are expert in this field. Specifically, I am asking you to prepare a statement in response to the following three questions which were prepared by the Economic Impact Sub-panel:

1. Will VHSIC exacerbate existing problems in securing an adequate supply of skilled manpower?

2. Will within firm allocation of manpower to VHSIC cause serious shortages of manpower on the commercial side of the industry?

3. Will the training of scientists and engineers be skewed into areas of minimal long-run payoff by university emphasis on VHSIC-related research? Conversely, will universities respond quickly enough to meet the manpower needs of the VHSIC program?

It would be of great help to the Panel in meeting its schedule if you (or an informed colleague) would prepare your reply such that it would reach me by Friday, September 5, 1980.

I certainly hope that you are able to find the time to participate in this important undertaking.

Very truly yours,

Norman G. Einspruch
Dean

NGE:nip

RESPONSES RECEIVED FROM

ALFRED J. STEIN, MOTOROLA
DAVID PACKARD
GORDON E. MOORE, INTEL
JAMES D. MEINDL, STANFORD ELECTRONICS LABORATORIES
CARVER MEAD, CALIFORNIA INSTITUTE OF TECHNOLOGY
EDWIN J. HILPERT, RACAL-MILGO
GEORGE H. HEILMEIER, TEXAS INSTRUMENTS
THOMAS E. EVERHART, CORNELL UNIVERSITY
LEWIS M. BRANSCOMB, INTERNATIONAL BUSINESS MACHINES CORPORATION
FRED A. BLUM, ROCKWELL INTERNATIONAL
JAMES M. EARLY, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

APPENDIX F

POSSIBLE FOREIGN REACTIONS TO THE VHSIC PROGRAM.

Purchase of Components. Foreign electronic concerns without an indigenous VLSI capability will be forced to buy more components from the United States or Japan. As more and more function is placed on each IC the semiconductor manufacturer will determine more of the cost of the equipment. The electronics manufacturer faces gradual loss of product control and will attempt to gain the VLSI capability either through vertical integration or through pressure on his government to create that capability in the country.

Internal VLSI Programs. The most likely reaction from some larger countries will be to intensify their internal programs. If the DoD VHSIC program remains on schedule, this is not likely to be an effective strategy on the part of any of the foreign countries except Japan. The experience and momentum already gathered by the U.S. semiconductor industry, when aided by the VHSIC program, will continue, and the technologies resulting from the program will be put to use commercially before other countries can make the same breakthroughs as long as the technology developed remains in this country.

Outright Purchase of Technology. A second likely reaction by foreign countries will be an attempt to buy U.S. technology, tools, companies, or all three. During the past several years this already has been taking place to the extent that there have been more than fifty equity purchases of U.S. semiconductor and semiconductor-related companies by non-U.S. interests (i.e., some semiconductor companies in the United States are now owned by French, British, German, Canadian, and Japanese electronics concerns). It is entirely possible that foreign-owned semiconductor manufacturers operating in the United States could obtain technology developed under the VHSIC program and funnel it to other countries both as technology itself and as manufactured components. This is true also of the specialized tools needed for the program.

Research and Development Incentives. Several governments offer incentives to multinational companies to carry out research and development activities within their respective countries. These incentives, ranging from tax credits to direct government subsidies covering more than half of the Research and Development cost, have been offered with the expectation that intensified local Research and Development will lead to increased local manufacturing activity and will serve to train native scientists and engineers. By comparison, from a tax standpoint, the United States has become one of the least favorable countries for private firms to practice research and development.

Israel, for example, has one of the most attractive Research and Development incentive programs. It has attracted large-scale IC design operations from two large U.S. companies. Others are considering similar Israeli operations.

Local research and development, fostered by such incentives, could be viewed by some governments as a means of attracting VHSIC-related activities to the local scene. For instance, local IC design centers could greatly decrease the time delay and working difficulties encountered in designing VLSI chips and applying chips in non-U.S. equipment applications. The advent of computer-aided design aids available on a time-sharing basis makes such design centers inexpensive to set up. This, together with appropriate tax incentives and subsidies, may prove a powerful inducement for U.S. companies to move major design activities abroad.

Hiring Experts. Yet another foreign reaction already practiced is the hiring of U.S. technologists. The British have attempted this on a large scale by setting up a VLSI company in the United States (INMOS). They presently are hiring people from U.S. industry to establish capability for the design and manufacture of VLSI products. The announced intention is to develop technology in this country and then to export it to the United Kingdom by setting up a plant there partially staffed at the professional level by U.S. expatriates. Other countries could be expected to take a similar approach once the VHSIC technology exists in this country.

Theft. Theft of technology also has become a real possibility. Hard evidence exists that such theft has occurred with or without the assistance of U.S. personnel. This practice is characteristic of some Eastern Bloc efforts and can be expected to continue.

Import Restrictions. In the past, some countries have applied restrictions on the import of ICs from other countries when the local industry had similar capabilities. It is entirely possible that this concept could be expanded to discourage importation of VHSIC parts into specific countries. In addition, non-tariff barriers (e.g., long and difficult qualification procedures, local purchase preferences, or long customs procedural delays) can arise. Banning importation of VHSIC devices into a particular country, however, whether by tariff or non-tariff means is considered unlikely. Local electronics equipment industries must have access to the most up-to-date components in order to remain competitive in their served world marketplaces. The consequences of a VHSIC product ban would have obvious serious consequences to any country not having a strong native VLSI industry (i.e., any foreign country except Japan).

Capital and Tax Incentives. All of the larger U.S.-owned commercial merchant market semiconductor firms have well established manufacturing facilities abroad. Capabilities include assembly, testing, and wafer fabrication. Factors such as government capital equipment grants, tax holiday, low labor costs, location inside tariff barriers, and intangible market benefits all figure in a U.S. company's decision to locate abroad.

The maturity of technologies utilized in these facilities varies from company to company with some manufacturers employing the latest developments and others, technologies that are three to five years old. Intracompany transfers of technology represent a possible leakage of VHSIC technology into foreign hands.

On the other hand, intracompany transfers of technology are subject to the same export restrictions that apply to any similar technology export. Since VHSIC technology is subject to munitions restrictions, the direct transfer of such technology abroad would be constrained. Indirect transfer of VHSIC concepts can occur through reposting of engineers from U.S. locations to foreign sites; however, this will be a sporadic process, much like the hiring of U.S. trained engineers by foreign firms. In the case of an intracompany personnel transfer, the individual and his technical ideas remain in the control of the U.S. firm.

The establishment by U.S. firms of facilities abroad will likely continue for all the reasons cited above irrespective of the VHSIC program. Direct transfer of VHSIC technology into such facilities is not expected to be a problem during periods of export restriction.

Foreign Situations

Japan. The original Japanese VLSI program was funded by a consortium of Japanese companies together with the Japanese government. Approximately $250 million were spent of which 40 percent were government funds. The MITI and the five participating companies established several laboratories to develop VLSI capability and applications. The program now is considered by most of the participants to have been only moderately successful. Charges are frequently made that the companies did not assign their most qualified people to work in the VLSI cooperative effort. Further, the participants from the various member companies often had difficulty sharing the information jointly developed. The original program has been completed, however, and a smaller MITI-based follow-on program is continuing. Although it is doubtful that the Japanese consortium realized the full direct benefit of its investment, the much publicized effort did focus the attention of Japanese industry on VLSI. As a result, Japan is the country most likely to compete with the U.S. capability for very-large-scale and very-high-speed ICs. Furthermore, Japanese semiconductor manufacturers have focused on the U.S. industry as their primary VLSI competitor. Further, it is anticipated that the Japanese semiconductor industry will seek and develop local support capability for equipment and raw materials to lessen dependence on U.S. supplies. Although the Japanese pose no direct threat to the military side of the VHSIC program, they are seeking to compete actively for commercial product business.

Japanese semiconductor company executives generally have expressed a lack of immediate concern for the competitive effects of the VHSIC program. The general belief stated is that Japanese industry as a whole has developed technology momentum and capacity at the critical time to propel it to a major world position in key types of semiconductors. The U.S. VHSIC program is seen as a reaction to the Japanese program, and it is perceived as being too late and too small to be a serious threat. The Japanese hasten to point out that their real goal is the electronic equipment industry (computers and telecommunications--not semiconductors) and that technology development is only one important factor in the competitive picture (other factors being timely capacity investment, dedication to quality, competent management, and dedicated employees).

West Germany. The West German government has supported advanced semiconductor development over a long period. The present program is funded at approximately $300 million and is administered through the Wissenschaftministerium (German NSF) and the Ministerium für Forschung und Technologie. So far support has been distributed to several native West German companies and universities. Siemens, the major manufacturer of semiconductors in West Germany, receives by far the largest share. The program is directed primarily not at military needs but at the telecommunication and computer industries.

United Kingdom. The United Kingdom through its National Enterprise Board has established a company (INMOS), initially organized in the United States to develop LSI production capability and products using a team of experts recruited mostly in the United States. The company will next set up a plant in the United Kingdom. With the change to the present Thatcher administration, the British government tried unsuccessfully to sell INMOS to a private U.K. company and more recently, after a lengthy debate, reluctantly provided INMOS its second-phase funding. As long as the Thatcher government endures, it is unlikely that INMOS will be a major factor in VLSI and that efforts to sell INMOS (even outside the U.K.) will continue.

Further support for the development of a U.K. semiconductor industry has come from the Department of Industry and Regional Development Boards. These boards are charged to encourage the development of local industry through capital equipment grants and other incentives. These grants are available to both U.K.- and non-U.K.-based companies operating in the region. Although the grants are not directed specifically to encouraging VLSI, many semiconductor manufacturers now operating in the U.K. (primarily Scotland) have concluded that expansion of their existing U.K. operations in high-technology areas is attractive.

The previous U.K. government under Prime Minister Heath developed a wide ranging program to encourage technical training and the application of microprocessor (MPU) techniques in U.K. electronic equipment. Although the program offered attractive incentives to equipment developers, it soon became controversial because British labor unions openly opposed LSI-based equipment on the basis that it eliminated jobs. The government incentive program is still in effect but not widely publicized.

Although the total U.K. support of native semiconductor activities (including INMOS and the MPU program) is funded at over $500 million over five years, key U.K. industry executives (with a few notable exceptions) are not alarmed by the failure of U.K. industry to develop LSI-VLSI capability. The VLSI impact appears not to be fully comprehended at this time throughout the U.K.-based suppliers. In addition, lack of capital for established firms to invest in very expensive facilities is cited as a strong reason to emphasize other semiconductor product areas.

France. The French government established both a VLSI technology development program and a program to develop a strong native semiconductor industry--Le Plan Circuit Integres--in 1978. The Plan Circuit Integres (PCI) is funded directly in the amount of $200 million over five years. Indirect investment by French industry, encouraged by promises of equipment follow-on business, has been substantial. At the encouragement of French government officials and prompted by the opportunity of qualification for French government electronic equipment designs (mostly in the telecommunications area) several U.S. firms (National Semiconductor, Motorola, and Harris) have elected to participate in assisting in the establishment of several French semiconductor companies. The PCI was established as a joint effort between several government ministries--the Post Telephone and Telegraph (PTT), the Ministry of Industry, and the military. As the best funded, the PTT and, to a lesser extent, the Ministry of Industry have dominated the program. Recently, the French military services have begun to feel left out. The semiconductor industry has been restructured through mergers and new company start-up activity to meet growing telephone component needs, and military programs have received less attention. The original intent of the French plan was to establish a native IC industry by acquiring advanced technology through establishment of joint ventures with appropriate foreign firms, rather than to develop new LSI technology. Recent discussions with French semiconductor executives have revealed that some of the sponsoring ministries may misunderstand the original intent and have become concerned about their special requirements. In particular, French military officials have expressed concern about the French program and point to the VHSIC program as "the right way to do it." Discussion of future programs will begin this year as the current program results are assessed and the follow-on program is formulated. It is reasonable to expect that the military will demand a much greater influence in any future program similar to the VHSIC program in the United States, citing as their reason the need for competitiveness of French military electronics.

Holland. Europe's largest semiconductor manufacturer, Philips, is headquartered in Eindhoven, the Netherlands. Although the capability of Philips in Holland is substantial, Philips also owns Volvo in West Germany, RTC in France, Mullard in the U.K., and Signetics in the United States, Philips' historical strength has been in consumer discrete and bipolar IC products. As a result of its internal computer needs, Philips has also developed high-speed logic capability. Philips executives acknowledge that their technical accomplishments in the MOS area are not as current, although

process capability is approaching current American standards. Product development of MOS memories and microprocessors has lagged behind that of the leading-edge U.S. companies; however, CAD is very sophisticated. The accomplishment of VHSIC objectives will not change the relative technological position of Philips, since it will remain in a catch-up mode.

The Soviet Union and Eastern Europe. The Eastern Bloc semiconductor makers do not actively sell their advanced products in Western markets. As a result, an assessment of Eastern Bloc capability is difficult, and published data on Eastern Bloc IC technology is sparse.

A recent trip by U.S. technologists through Czechoslovakian semiconductor plants revealed device capabilities five or six years behind those current in U.S. industry. Interviews with a Russian emigre formerly employed in the Russian semiconductor industry confirmed that the civilian products are built using technology at least that old. However, the informant also indicated that military products were built in entirely separate lines by separate staffs and were of much more modern construction. Visitors to Soviet semiconductor plants early in 1979 were given samples of allegedly Russian-built 16K RAMs and ECL logic. Although the origin of the parts is not definitely known, the supposition must be that the Soviets are at, or near, the representative technical sophistication in their more advanced facilities. Occasional references appear in the press to Eastern Bloc copies of U. S. designed microprocessors; however, the existence of these MPUs is unconfirmed. East-West technology exchanges involving consenting companies do not appear to have been an important factor in Eastern Bloc technology advancement outside of Yugoslavia. The former Russian semiconductor engineer did mention the existence of a group of "consultants" who could obtain answers to most questions about Western technology in a matter of months. VHSIC technology can well be expected to be a target of these "consultants'" activities.

The rate of advancement of Soviet and Eastern Bloc military IC capability must be presumed to be rapid, as solid-state electronics is a major target area for Russian technology development. Continued progress such as VHSIC is necessary if the United States is to retain its lead in military electronics.

People's Republic of China. China is sometimes seen by U.S. semiconductor industry observers as a potential latter-day Japan. The Chinese government has embarked on a major economic revitalization program characterized by the "Four Modernizations": agriculture, industry, national defense, and science and technology. Particularly in the science and technology area, the Chinese are engaged in a "great leap outward" seeking to understand, acquire, and use non-Chinese ideas. Semiconductor ICs are seen as a key element of science and technology needed for the electronics necessary to upgrade all phases of Chinese life. As a result, Chinese visitors to the United States, Chinese students in the United States, and questions asked of U.S. visitors to China all show a strong interest in semiconductor technology. Some Chinese electronics engineers now are being trained by Western semiconductor firms to do SSI and MSI design engineering.

Although on the surface there may seem to be parallels between Japan in 1946 and China in 1980, in fact the Chinese face far more formidable problems. The gap in training of qualified engineers during the 1966-1971 Cultural Revolution, the extreme backwardness of the industry and laboratories, the lack of the highly sophisticated infrastructure needed to support an IC industry, the lack of foreign exchange with which to purchase raw materials, the high cost of manufacturing equipment and technology abroad, and the determined resistance of some Chinese Communist Party cadres to modernization programs based on non-Maoist principles all combine to make progress in sophisticated technologies slow. The Chinese are taking advantage of every scrap of information available from the West in journal articles, visits, exchanges, and educational opportunities. Although some laboratory facilities, such as those at Qinghua University in Beijing, have produced remarkable results with the small wafers and limited equipment available, the technology in use is far from production ready. Even with the aid of foreign technology purchases, the diversity of problems facing the Chinese semiconductor industry is so broad that a quick solution does not seem possible.

VHSIC technology is well beyond the reach of Chinese industry. Even if such technology were to be made available, the capability to use it effectively is lacking for all but isolated laboratory results. Furthermore, development of the chemical, equipment, and technical bases and facilities needed to support a VLSI industry will take a long time, not to mention the changes in social and economic life and the attitude of party cadres toward the "four modernizations."

The pace of technical change in VHSIC-related fields remains rapid. Thus, the Chinese will do well just to hold their present technological position relative to the state of the art, VHSIC or no VHSIC.

Other Countries. Italy, Korea, Finland, Spain, Israel, Austria, Taiwan, and Ireland all have some government-supported programs to assist native semiconductor industries. None of these are expected to change the balance of power in the VLSI industry.

CONCLUSIONS

With the exception of the Japanese VLSI Cooperative Association and an effort by NTT in Japan, VLSI foreign-government-supported programs as they are presently planned will not change the international competitive balance of trade. The Japanese plans, however, are following the same path as the previous successful Japanese joint industry-government efforts to build the automotive, consumer electronics, and steel industries. The Japanese computer plan has yet to be completely successful, but effort is continuing in areas such as VLSI. With or without government support, however, the Japanese semiconductor industry is very capable, with fine, competitive products.

The other foreign-government-sponsored VLSI program face a poorer prospect for success. Many countries desire a strong semiconductor industry but do not have the internal market demand necessary to adequately support a native industry. Most government supported semiconducter programs are based on assumptions of substantial sales to other countries--usually countries with their own government plan. The prospects of substantial success are unlikely, particularly when seen in the context of previously weak or nonexistent national capability.

The battle for share of the VHSIC/VLSI market will be fought in the United States and in Europe between the U.S. and Japanese suppliers. The VHSIC program is likely to strengthen the United States nonmilitary component and electronic equipment capability to engage in this fight.

APPENDIX G

LIMITATIONS ON DESIGN AND PERFORMANCE OF INTEGRATED CIRCUITS

Prepared by R. B. Bate and P. K. Chatterjee

In this appendix some of the limits on the performance and on the possible extent of integration of logic devices imposed by constraints ranging from general physical laws to the state of the art of materials, fabrication, and process technology will be examined. Although these limits are beyond the goals of the VHSIC program, it is instructive to examine them in the context of DoD systems for several reasons:

1. In the absence of concrete intelligence, truly fundamental laws can place hard limits on the ultimate system performance potentially achievable by an adversary, even in the event that he develops device technologies unknown to us.

2. Fundamental limits serve to alert the user to potential new failure modes that may become observable as performance is improved.

3. Such considerations can assist in gauging the difficulty of achieving certain performance goals by virtue of the proximity of these goals to ultimate limits.

The hard thermodynamic and quantum limits on performance that should hold regardless of the materials and technology employed will be discussed first. The limits more closely related to specific VHSIC technologies then will be examined.

DEVICE LIMITS THAT ARE INDEPENDENT OF MATERIALS AND TECHNOLOGY

Fundamental limits on device performance have been explored theoretically by means of abstract models.* A particle (electron) in a two-valley potential has been used to explore the thermodynamic limits and

* A review of this work will appear in N. G. Einspruch, Editor, Microstructure Science and Engineering/VLSI, Vol. 4, Academic Press

a simplified version of this model has been employed to determine quantum limits. The results of these studies can be summarized as follows:

1. Thermodynamics places a lower limit of order kT (= $4 \cdot 10^{-6}$ fJ at room temperature) on the energy, E, required to perform a single logic operation. This includes only the energy dissipated in the gate itself. This low value of E, which can be thought of as the minimum possible power-delay product per logic gate, is attained if the switching time, t_s, is very long compared to τ, the energy relaxation time of the model particle in the potential well. However, since thermodynamics alone places no limits on τ, no further thermodynamic limitation on power-delay product applies.

2. Quantum mechanically, the uncertainty principle gives the often quoted result:

$$Et_s \gtrsim n \sim 10^{-19} \text{ fJ-sec}.$$

It is important to note, however, that when E or t_s approach values such that this inequality becomes an equality, the probability of an error is of order 1/2 (i.e., the gate is totally unreliable). Thus, more stringent limits exist for reliable operation of the gate. Analysis of simple abstract model gives the more useful approximate relation:

$$Et_s \gtrsim h\ (2/\pi)\ [\ell n(5/P_e)]^2,$$

where P_e is the probability of finding the logic gate in the incorrect logic state. For a chip incorporating N_g gates operating at a soft error rate of R_e, this leads to a minimum chip power dissipation of:

$$P_{chip} \gtrsim 6.7 \cdot 10^{-35}\ f_c\ (FTR)\ [\ell n\ \ (5\ FTR/R_e)]^2 \text{ watts},$$

where FTR is the functional throughput rate in gate-Hz. Conversely, for a given power dissipation and throughput, this equation predicts the minimum realizable soft error rate regardless of technology employed.

The limits predicted so far take into consideration only the minimum energy that must be dissipated in the logic gate itself. Many have argued that, at least for asynchronous logic, the operation of a random logic gate implies dissipation in some external driver of energy equivalent to the potential energy difference or barrier between the two logic states. It is also difficult to conceive of a useful synchronous system that does not also require this. If this view is adopted, then the picture changes as follows:

1. Thermodynamics requires that the minimum total energy dissipation required per logic gate operation is:

$$E_T \sim 2kT\ \ell n\ [(1-9_e)/P_e],$$

which for reasonable error rates is certainly no more than 100 kT.

2. The quantum mechanical requirements also change.

The total minimum quantum mechanical energy requirement, assuming that the potential energy separating the two logic states must be dissipated in order to selectively change the logic state of the gate, is:

$$E_T t_s \gtrsim - \bar{n} \, (2/\pi) \, 103 \, \ell n \, (11.6 \, P_e),$$

leading to a minimum required power dissipation of:

$$P_{chip} \gtrsim -6.9 \cdot 10^{-33} \, (FTR)^2 / N_g \quad \ell n (11.6 \, R_e / FTR).$$

The foregoing equations are used to illustrate the proximity of the VHSIC goals to fundamental technology-independent limits in Figure G-1. A gate count, N_g, of 10^5 gates/chip has been assumed and an error rate of $2.8 \cdot 10^{-13}$ sec corresponding to one failure in 10^9 hours of operation has been assumed. If the chip incorporates single-bit error detection and correction, this would be the approximate chip failure rate assuming that the chip contains one defective gate. It is apparent from Figure G-1 that these technology-independent limits have little impact on VHSIC goals.

More specific models that are not necessarily technology independent can be employed to predict less remote limits. However, no fundamental limits which constitute a threat to VHSIC goals have been identified.

TECHNOLOGY INDUCED LIMITS TO CIRCUIT INTEGRATION

Technological limits to integration derive from material constants, fabrication techniques, and electrical parameters. The constraints imposed by these considerations can sometimes be circumvented by the use of structural changes, new materials, lower operating temperatures, and other forms of device and circuit cleverness. Materials constants include electrical and thermal conductivity, mobility, dielectric constants, saturation velocity, and dopant solubility. Limits associated with fabrication technology involve doping variation, processing radiation, defects, layer thickness uniformity and pattern edge roughness, process bias and tolerance, and total heat cycle (diffusion coefficient-time product). Constraints relating to electrical parameters include oxide and junction breakdown tunneling, hot electron injection, avalanche multiplication, punchthrough conduction, and small geometry effects. These parameters and their specific effects on various IC technologies are dealt with in the following sections. The implication of nuclear radiation in the form of alpha particles or cosmic rays also is presented. Technical concerns indicate a practical lower limit on feature size of about 0.1 to 0.4 μm for IC applications.

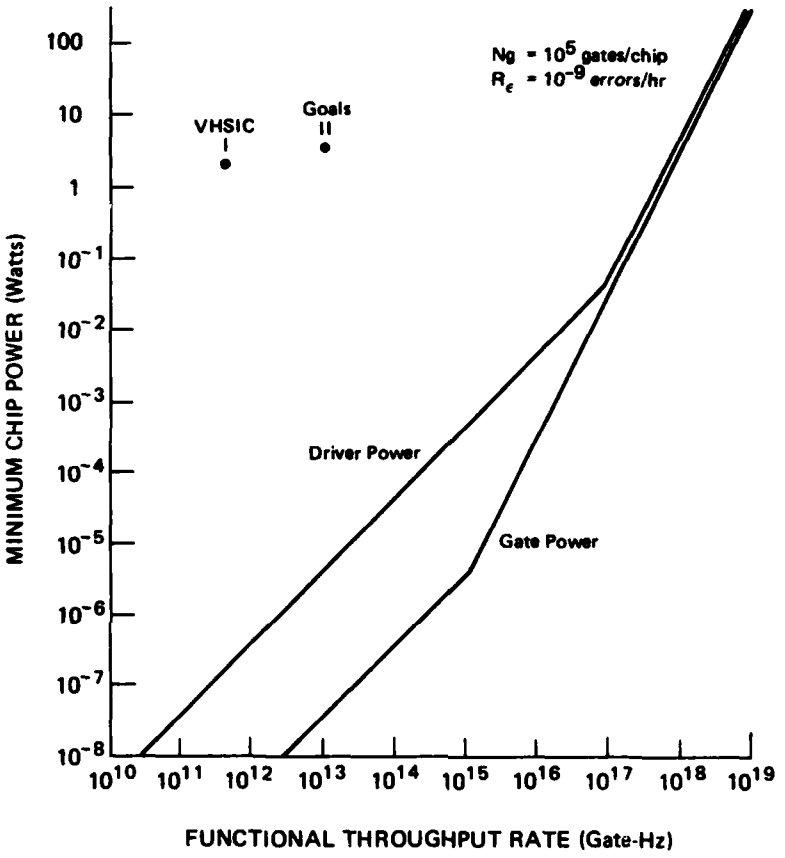

Figure G-1. Technology - independent thermodynamic and quantum limits on logic chip performance.

INTERCONNECTION AND DEVICE-ISOLATION-INDUCED LIMITS

As device geometries are reduced and more circuit functions are integrated on chip, circuit performance tends to be limited by interconnect time constants. At the VLSI complexity of integration, design approaches must be modular to manage complexity. The signal-propagation delays between modules thus determine the performance of the overall circuit. Typical 16-bit MOS microprocessor designs have 30 percent of the area occupied by interconnections and the I^2L version has 70 percent of its area occupied by interconnect. This trend is expected to continue and the role of interconnect design in VLSI circuits will become as important as that of waveguides in microwave design.

Capacitance Scaling. The parallel plate model of capacitance of interconnect lines breaks down for interconnects with linewidth, w, comparable to dielectric thickness, h. For such structures, microstrip line theory may be used to determine the role of fringing effects and coupling to adjacent lines. The self-capacitance of an interconnect line is important in determining the speed performance of a circuit. However, in logic application, it is necessary to run a series of lines parallel to each other so that line to line mutual capacitance considerations must be invoked with noise margin requirements as a constraint.

Figure G-2 compares, as a function of interconnect linewidth, w, the capacitance per unit length of interconnect for two insulating substrate types (SOS and GaAs) with that of a 1-μm SiO_2 on a conducting silicon substrate. The calculations assume a line to line spacing of 1.5W. It is interesting to note that the high dielectric constant of the thick insulating substrate results in a capacitance scaling which is logarithmic with the line width. The mutual capacitances shown as a band in Figure G-2 cause greater noise margin problems in the insulating substrates than in the conducting substrate, which essentially provides a ground plane.

It is important to note that, in the submicron regime, the capacitance per unit length does not scale, and if the chip dimensions are held constant, intermodule signal transfer time will scale only by the scaling of the RC time constants of the lines that connect the modules. Since the resistance at small dimensions will increase with scaling, the time constants may actually increase.

Line Resistance. The use of interconnection layers with sheet resistivity greater than 1 ohm/sq has been ruled out for performance requirements in 1-μm technology. This eliminates the use of polysilicon or refractory silicides as interconnection layers at submicron geometry. The topological requirements for high-density circuit connection will dictate

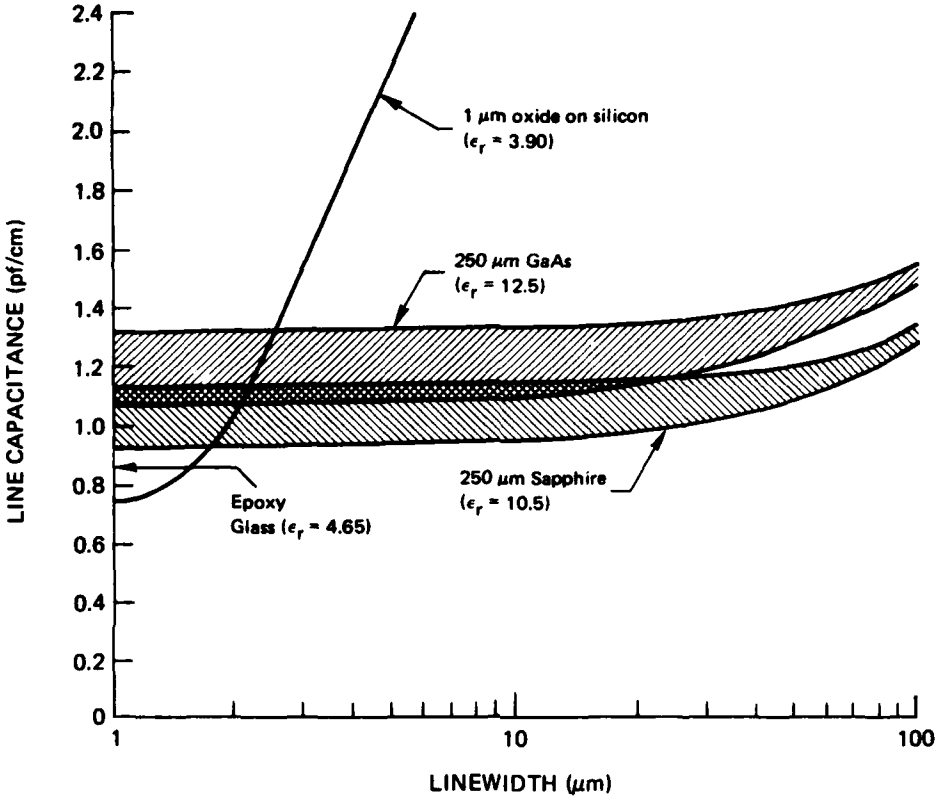

Figure G-2. Comparison of capacitance per unit length of interconnect of SOS and GaAs with that of 1 μm SiO_2 on a conducting silicon substrate as a function of interconnect linewidth.

multilayer metal interconnect where the choice of metal will be dictated by the requirement of interlevel passivation. It is reasonable to expect metal resistivities of 5 to 10 μohm.cm which will limit propagation delays to greater than 1 ns/cm of interconnection. Thus, modular designs for chips that are many millimeters in dimension will be limited by RC delays so that the source resistance of the device (switch) has little or no influence on the overall circuit speed.

Device Isolation Limits and Lateral Diffusion. The ability to isolate devices on a single substrate resulted in the conception of the integrated circuit. It is constructive, therefore, to re-examine this issue in the context of VLSI and VHSIC. Isolation techniques that have been successful in the LSI era are based mostly on local oxidation of silicon using silicon nitride as the oxidation barrier for the active region. The "oxide isolation" scheme is preferred to junction isolation schemes purely on the basis of leakage in reverse biased junctions. Oxide isolation schemes practiced today lead to finite transition regions from active to passive sections. This transition region consumes a significant portion of the chip area at scaled dimensions if the field oxide is not scaled for capacitance reasons.

Apart from the physical encroachment of the device boundary caused by a finite transition region, the long oxidation process generates point defects that propagate into the silicon causing an enhanced lateral diffusion of the dopant species in the vicinity of the isolation edges. This enhanced lateral diffusion results in an additional encroachment of the physical boundaries of the active device, thus limiting the minimum active dimension to about three times the isolation oxide thickness.

Electromigration. It has been shown that intermodule interconnects as long as the chip dimensions will be dominated by RC delay so that increasing current density will not increase circuit speed. For shorter interconnections, it is possible to reduce the resistive loss such that an increased current drive produces an increase in circuit speed. The limit to such an increase is dictated by electromigration at high current density in scaled wiring. At geometries below 1 μm, grain sizes for aluminum-based interconnects once again become comparable to line width, increasing the probability of electromigration-related failures. The study of refractory and intermetallic layers under way currently may provide some interconnect structures in which the MTBF for electromigration may be improved. For short interconnection, however, the limit to increase in speed will be the current density in the interconnect. Based on this limit, and the logarithmic scaling of capacitance, the performance increase between silicon and GaAs devices, for example, is marginal.

Limits to FET Scaling for Integrated Circuits

Device Scaling Laws for Circuit Applications. The primary factors that limit the size of MOSFETs are junction and oxide breakdown and hot electron effects. If we examine the intrinsic FET, the simple scaling laws proposed by Dennard and co-workers (1974) require a linear downscaling of oxide thickness and voltage with dimension with a simultaneous upscaling of channel doping, in an attempt to minimize the increase of electric fields. Since the source drain junctions are cylindrical rather than planar, the breakdown voltage at the junction is rapidly decreased with increased channel doping to limit the operation of the MOSFET. This drain breakdown limit is near fundamental for the operation of the FET itself. Further, the voltage scaling is restricted by the following considerations in real IC applications and noise margin requirements for full temperature operation and process tolerances:

1. Parameter nonuniformity due to material and geometry variation.

2. Electrical crosstalk due to capacitive coupling on clock lines.

3. Parasitic feedback due to source/drain resistors formed by shallow n+ junctions.

4. Finite capacitance of the inversion layer.

5. Reduction of effective mobility due to impurity scattering for heavy channel doping.

6. Drift velocity saturation in the channel and hot carrier effects.

7. Subthreshold leakage that does not scale and becomes increasingly severe in military environments.

8. Oxide integrity considerations that limit the downscaling of gate oxide.

Based on these considerations, scaling of MOSFETs should follow a non-linear law to include all the above considerations. Table G-1 shows a quasi-constant voltage scaling law employing a slow variation of oxide thickness and voltage to compensate for the above effects. Using a short channel MOSFET model, one may calculate the effective drive current (Figure G-3) in saturation as a function of scale factor based on this scaling law and compare it to Dennard's constant field scaling law. The effective drive current is normalized by the voltage scaling factor. This current represents the available drive capability for MOSFET circuits where the basic performance factor is the charging of capacitance. The drive capability for a constant field scaling decreases below 1 μm, as the effective mobility is reduced due to impurity scattering. This reflects an

actual decrease in real performance for MOSFET circuits fabricated based on constant field scaling for gate lengths below 1 μm. Under the quasi-constant scaling law, the performance peaks at L ∿ 0.3μm for p-channel devices. These are limits which are set to reflect the particular choice of the scaling parameters. It is possible to choose a different functional form for this scaling law to shift the peak performance limit. The point of interest is that as long as all the circuit-related effects are included in the scaling laws as monotonic functions, the maximum performance peak exists. Physically, the limit is set by the condition that the parasitic RC elements dominate the circuit response in spite of very high intrinsic device speed. The device speed itself is limited by carrier velocity saturation and by the finite inversion channel capacitance or thickness which limits the effective gate capacitance and transconductance. Thus, although intrinsic device propagation delays of approximately 100 to 200 ps with a power dissipation of approximately 0.5 ∿w are possible, circuit speed for VLSI complexity probably will be limited to approximately 0.5 to 1.0 nsec time delay. It is interesting to note that the drift velocity saturation causes the n-channel and p-channel devices to have similar drive capabilities at very short lengths (L <0.3 μm).

Table G-1. Definition of Scaling Law

Scaling Law	Constant Field	Constant Voltage	Quasi Constant Voltage
Dimensions (λ)	λ	λ	λ
Gate oxide (λ_o)	λ	$\sqrt{\lambda}$	λ
Doping (λ_N)	λ	λ	λ
Voltage (λv)	λ	1	$\sqrt{\lambda}$

Full scale ($\lambda = 1$) values of L = 3 μm; L_α = 500A; $N_A = 2.5 \times 10^{15}$ cm^{-3}, are used.

High Field Effects and Reliability Issues. The maximum performance of scaled MOSFETs is obtained when the operating conditions approach very high fields in silicon, and operating the device close to breakdown leads to long-term drift caused by hot electron injections into the gate oxide, leading to a shift in threshold voltage. The weak avalanche multiplication causes a majority carrier current in the substrate leading to self-biasing, and a secondary ionized minority current, which can diffuse to neighboring high impedance nodes and cause memory errors or logic transitions. These effects have been observed under electric fields only slightly greater than 1 volt/μm and can cause severe design and reliability problems in MOSFETs.

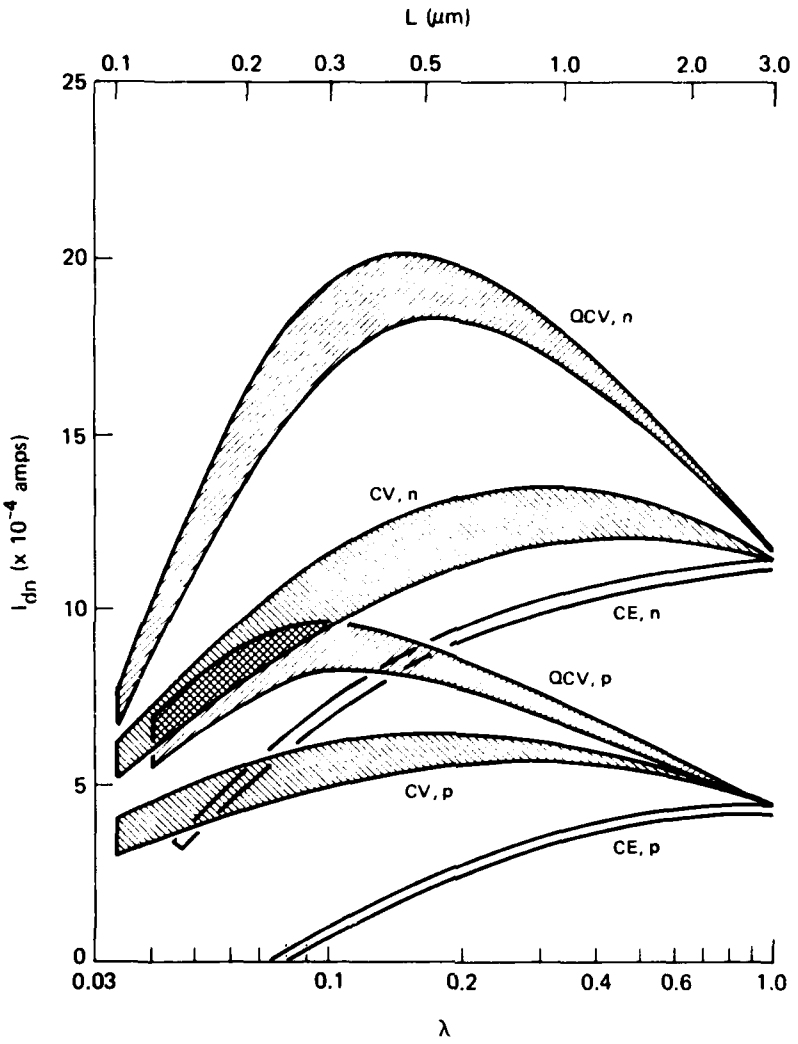

Figure G-3. Effective drive current in saturation as a function of scale factor.

At this point, it is interesting to note that the ionization coefficient for holes in silicon is approximately 100 times lower than that of electrons, so that the impact ionization current in p-channel devices is much lower than that in n-channel devices. Further, the Si/SiO_2 valence band barrier (approximately 3.6 eV) is larger than the conduction band barrier (approximately 3.2 eV) so that the net probability of hot carrier injection into the gate oxide is significantly lower for p-channel devices than it is for n-channel devices.

Complementary versus Single Carrier Technology. The choice of single carrier versus complementary MOSFET technologies for circuit applications is related to a three-way tradeoff between process complexity, power dissipation, and design cycle time. Complementary technologies traditionally have required a more difficult fabrication procedure involving the fabrication of p-n-p-n structures in the case of bulk CMOS, which could potentially lead to SCR type latch-up in circuit operation. The long channel 3:1 drive capability ratio of p-channel and n-channel devices has also required a density penalty for CMOS circuits. However, at submicron device lengths, the drive capabilities of the p-channel and n-channel devices are similar, as established above. The issue of power dissipation in circuits has been addressed by dynamic circuit design, or by selective power-up techniques in nMOS memories. Both approaches require multithreshold devices (typically, three to four different threshold voltages are common in LSI memories), which increase the process complexity for single-carrier nMOS technologies. Further, the power dissipation requirements are very stringent so that each gate must be optimized to drive its dedicated load to minimize active power dissipation. On the other hand, CMOS circuits may use over-designed gates since the gates have an automatic power-down feature dictated by subthreshold current. In terms of large designs, the design cycle time for CMOS devices is thus drastically reduced. However, the major problems in bulk CMOS technology are associated with SCR latch-up which depends on the impact ionization induced majority carrier leakage in each device. The option of insulating substrates is undesirable in circuit applications for sapphire-like substances since the decrease in load capacitance for submicron lines is dominated by fringing effects so that the circuit performance is dictated by the available carrier mobility in the epitaxial silicon. Silicon-on-insulator substrates using laser annealing technology may provide acceptable quality substrates for CMOS fabrication. If these substrates are available, design with complementary carriers allows maximum exploitation of device capabilities in an integrated circuit environment.

MESFET Technology. The silicon MESFET is based on the field effect control of majority carrier current by using a metal semiconductor (Schottky diode) junction in contrast to the insulating gate used in MOSFETs. Silicon MESFETs have not been used for LSI applications since they are inherently limited to low voltage operation. For submicron circuits, however, MOS scaling dictates lower operating voltages, and the MESFET technology offers an alternative to thin insulating oxides. In the comparison of technology-induced limits on FET technology, the MESFET

offers some potential advantages. The absence of the thin insulating oxide removes the reliability problems based on charge trapping in insulators or gate oxide wear-out considerations. Limits to operation set by parameter control in MOSFETs which relate to thin oxide, however, simply translate into problems of controlling a Schottky barrier height. The MESFET technology can provide packing density and performance very similar to nMOS technology in all other respects.

The major advantage of submicron MESFETs in a military application is that they offer a radiation-hardness level comparable to bipolar technologies with a packing density comparable to nMOS technology.

Limits to Bipolar Scaling for Integrated Circuits

In contrast to the FET technologies, no simple scaling laws can be established for bipolar devices because of their complex three-dimensional nature. Since bipolar devices are current-controlled, operating voltages do not affect their performance as much as for FETs. The base-emitter-threshold is set by a p-n junction contact potential which is more invariant to scaling. However, the maximum collector base voltage of the device is set by the collector breakdown condition which is similar in order to MOSFET maximum voltage. The closed geometry required for bipolars results in wasted annular regions which contribute only to performance degradation for the bipolar device.

Among the several factors that limit the performance of bipolar switching transistors, the more significant ones are the emitter-collector transit time and the emitter-injection efficiency. The emitter-collector transit time is rather fundamental and represents the smallest delay time a transistor can have if the transistor also has sufficient emitter injection efficiency. This transit time is defined by:

$$\tau_{ec} = \tau_E + \tau_C + \tau_C' .$$

In the above expression, τ_C' is the collector charging time and may be neglected in a well designed transistor. τ_C is the collector depletion layer transit time, which would contribute approximately 0.5 ps delay time for every 1000 Å depletion layer. τ_B is the base transit time, which relates to base width. τ_E is the emitter depletion layer charging time, which relates to emitter current as well as emitter base, C_e, and collector base, C_c, junction capacitance.

When the neutral base width becomes comparable to the carrier mean free path, carriers experience very few collisions within the base. At this limit, the transport process tends to thermionic emission and the scattering time is finite and must be accounted for in the Boltzman

transport equations. The mean free path of the electrons for a saturated drift velocity of approximately $2 \cdot 10^6$ cm/s is about 40 to 50 Å. When the base width becomes comparable to several mean free path lengths, and detailed calculations indicate that for basewidth W ≈ 200 Å, significant thermionic emission occurs. The base transit time, τ_B, for a n-p-n silicon transitor with 10^{18} cm^{-3} base-doping, $\tau_B = W_b^2/2D_b$ becomes 0.4 ps in this limit so that the base contributes little to delay time.

The emitter time constant, on the other hand, is dependent on emitter current and is therefore dictated by power dissipation considerations. Thus, for a chip dissipating 10 W/cm^2 with a IV power supply in which 1 percent of the wafer area corresponds to the emitter, the current density in the emitter is 1 KA/cm^2, and for 10^{18} cm^{-3} base doping, to calculate the junction capacitance, $_E = KT/qI_E$ $(C_e + C_c)$ = 26.5 ps. Thus, the speed of bipolar devices is current density limited due to practical problems of heat dissipation in IC environments and more acute problems of electromigration failure of metal interconnects. Under the above conditions, the speed power product of bipolar transistors with 1- m emitters is .25 fJ.

To be useful in a switching circuit, the bipolar transistor also must have sufficient current gain. The common base current gain of a bipolar transistor is dependent on the emitter injection efficiency, y, which is dependent on several factors that are important to a shallow junction transistor and can be expressed by:

$$1/\gamma = 1 + \exp(q\Delta V_g/kT) \cdot (N_B/N_E) \cdot (D_e/D_b) \cdot (W_b + D_b/V_s)/(W_C + D_e/S_c).$$

In the above expression, V_g is the bandgap narrowing due to heavy doping, which is in the neighborhood of 150 mV for modern shallow junction devices. The factor, D_b/V_s, adds to the base width about 100 Å and can be neglected except for extreme cases. The factor D_e/S_e (S_e is the emitter surface recombination velocity) can be quite important at shallow junctions below 2000 Å and will be the most difficult challenge in scaling bipolar technology. If materials related problems of using heterojunction emitters can be overcome, the emitter injection efficiency problem could be significantly resolved.

So far, the discussion has been limited to the simplest I^2L structure. Structure modifications, such as double-diffused injector, substrate injector, polyextrinsic base and Schottkys, have been implemented on full-size devices to obtain significant performance gains without scaling. The question is how easily can these structures be scaled to submicron geometries. There are no basic problems with the double-diffused and substrate injectors. Using the present technology for growing poly and good quality epi simultaneously, the poly grain size may be of the order of the minimum linewidth or larger, which would present a problem in terms of patterning and metal coverage. The doping levels (approximately 10^{18} cm^{-3}) required for submicrometer geometries would make the fabrication of good Schottkys difficult; however, isolated Schottsky could be used in critical paths and I/O without seriously impacting chip area.

Circuit Performance Limits for I^2L and Its Modifications

The above discussion of device performance limits was applicable to the simple I^2L devices where device scaling has been incorporated. Structural modifications, such as double diffused injectors, substrate injectors, poly-extrinsic based, and Schottsky, have been implemented in unscaled devices to obtain significant performance gains without device scaling. The question is how easily can these structures be scaled to submicron devices. Double diffused approaches are limited by coupled diffusion problems at the higher doping density required for scaled devices. In the case of poly-extrinsic base devices, present epitaxial techniques will be limited by polysilicon grain width which may present patterning and metal step coverage problems. The base doping levels approximately 10^{18} cm^{-3}) required for 0.4 to 0.5-μm devices will result in unacceptable barrier heights and reverse leakage in Schottky barrier devices. Since high current levels are inevitable in bipolar technologies aimed for high speed, semiconductor contact resistance will play a major role in limiting bipolar VLSI circuit performance.

Tolerance to Environment

As we approach geometry sizes, circuit operation depends on a very small quantity of charge flow, especially for FET memory devices. It was recently discovered that dynamic memory devices can be susceptible to errors due to radiation from traces of radioactive elements in package materials that emit alpha particles. These alpha particles generate approximately 10^6 electron hole pairs to a depth of approximately 25 μm as they come to rest in the silicon. The diffusing electrons are responsible for discharging cell capacitors in dynamic RAMs. Static memories were thought to be immune to such radiation, but power dissipation limitations have now led to design of static cells with holding currents in the nanoamps range. Since the diffusing current due to alpha particles is equivalent to approximately 10 to 100 μA for a short time, these memories are also vulnerable to error.

As memory sizes grow, this error level will be intolerable since other cosmic radiation will also affect the memory. It is thus a major challenge to design memory elements that are largely immune to alpha particles. Recently a novel dynamic RAM structure, the taper-isolated RAM (TIRAM) cell, has been proposed that has the novel feature--radiation-induced carriers generated outside a shallow (approximately 2000 Å) surface layer are not collected in the surface data storage region. Thus, for example, a 100 ns γ pulse of 10^7 rad (silicon) will create a collected carrier density of only about 10^9 cm^{-2} which will produce a temporary signal voltage shift of approximately 2 mV for a 500 Å gate oxide thickness, compared to a signal of 2 to 3 volts.

The design of VLSI memory will require such innovative device structures to cope with the environmental noise which, for today's memory structures, will totally dominate over the available signal.

REFERENCE

R. H. Dennard et. al., IEEE Journal Solid State Circuits SC9, 256, 1974.

APPENDIX H

Abstract of remarks by Dr. Larry Hansen, President,
Industries Equipment Group, VARIAN,
speaker on behalf of the Semiconductor and Materials
Institute (SEMI) as presented to the committee on June 19, 1980.

The United States semiconductor manufacturing equipment industry states that it is well tuned to the needs of the semiconductor device industry and that, ultimately, critical manufacturing equipment will be developed to meet the needs of the device industry as it moves into the era of VLSI devices and VHSICs. This will happen with or without the DoD VHSIC program.

However, there are some critical issues and some questions that must be answered relative to this critical process and test equipment. Pertinent questions are:

1. Who will develop this equipment?
2. How long will it take?
3. How much will it cost?
4. To whom will it be available (and under what conditions)?

A great deal depends on how these issues are resolved for the answers will have a major impact on the VHSIC program and the ultimate success of that program.

In the United States, there are about 275 companies in the semiconductor manufacturing equipment business. Most are relatively small companies. About 60 percent have sales of $5.0 million or less, and 95 percent have sales of $50.0 million or less.

The largest are around $100 million per year. These are sales in semiconductor manufacturing equipment only. Some companies are also in other business areas. The United States' industry is ahead of competing industries in Japan and Europe.

Manufacturing equipment is to a large extent the gating item for new generations of devices. Several significant advances must be made to achieve the objectives of the VHSIC program. This is well known by our overseas competitors. The Japanese government in their VLSI program put a large amount of money into equipment development.

1. Toshiba developed an E-beam system.

2. Hitachi was given funding to work in several areas. For example, they have been doing basic work on ion implantation for three years.

3. JEOL has developed an E-beam system.

4. Nissin High Voltage is working on ion implantation. They took a license from Western Electric.

The Japanese have made one big mistake--they gave the equipment development funds primarily to device companies. For all the money spent, they did not develop an equipment industry. That error is recognized by the Japanese device and equipment people. They will not make that mistake again.

The same is true in Europe. Each country is funding equipment-development programs. Each has a different approach to the problem, but the problems are becoming well recognized.

When the VHSIC program was first conceptualized, it was recognized that there were some critical equipment technologies that required up-front support to make certain that the technology would be available when it was needed. Somehow, the program seems to have lost sight of some of those critical needs.

The semiconductor manufacturing equipment industry is composed of relatively small companies. Most have small numbers of highly qualified scientific people and they spend between 10 and 15 percent of sales on new product development. There are very few industries in the world today that get more "bang for the buck" spent in R&D than the U.S. semiconductor manufacturing equipment industry. These small companies are for the most part well managed, dynamic companies who have come a long way in a short period of time. However, most of these companies are growing very rapidly, and they are underfinanced to handle the growth.

There is much concern about the so-called increasing capital intensity of the semiconductor industry, and the impact this high-cost processing and testing equipment will have on the device companies. A point that is mostly missed is the enormous increases in costs related to the development of this new complex equipment.

It takes $200,000 to develop a piece of $20,000 processing equipment and get it into limited production. It takes $20 to $30 million to develop a piece of $1.0 million equipment and get it into limited production. This high equipment development cost contributes significantly towards the ultimate price of the equipment to the semiconductor companies.

As an example, consider some specific parts of the lithographic process, which is recognized to be one of the major sticking points in the technology required to reach the VHSIC objectives.

Shown in Figure H-1 are the present and future status of the semiconductor process sequences, described in terms of the exposure method. The bulk of devices today are made using the steps shown in the boxes on top. However, with the E-beam mask-maker and the direct-stepper, two micron geometry devices are practical in production. Actually, this diagram is a bit behind the times, and an E-beam reticle generator is now available. In three to four years, sub-micron geometry capability will be available using E-beam-generated masks with X-ray exposure systems and/or E-beam on direct-write machines.

Shown in Figure H-2 are some parameters associated with these equipments. These data were generated by General Instruments. Shown are typical resolutions, alignment capability, expected throughput numbers, and estimated prices.

Available are some specific numbers based on Varian's position in this business which may be useful to help put things in the proper perspective. At the present time, Varian has an E-Beam mask-making machine, based on the original Bell Telephone Laboratory Technology. This machine now offers the most cost-effective method of making high-quality masks and reticles available today.

They plan to get a sub-micron mask and reticle-maker and, ultimately, a direct-write E-Beam machine. To get from where we now are to that production direct-write E-Beam machine will take approximately 200 man years of R&D and manufacturing support effort. The cost of this effort will be about $12.0 million. Varian plans to spend the required money to meet these objectives. Varian has asked to participate in the VHSIC program because they would like to reduce the time for this development program. With DoD participation, they feel they can reduce the time to make the equipment available on the desired VHSIC schedules.

In addition to Electron Beam Lithography as an example of a process requiring significant investment in capital equipment development to bring it to the level where the requirements of the VHSIC program can be met, there are several others.

1. Much work has been done by way of developing equipment for dry etching processes, but a good bit more needs to be done to achieve processes consistent with the requirements of VHSICs.

METHOD	RESOLUTION (μm)	ALIGNMENT (μm)	TYPICAL THROUGHPUT (WAFERS/HR)	APPROXIMATE PRICE
SCANNING, 1:1 OPTICAL PROJECTION	2 (LOW VOLUME) 2.5-3 (PRODUCTION)	± 1	60	$150,000-200,000
SCANNING, 1:1 OPTICAL PROJECTION, DEEP ULTRAVIOLET	1-1.5 (NOT COMMERCIALLY AVAILABLE)	± 0.25	60	300,000
DIRECT-STEP-ON-WAFER, OPTICAL W/E-BEAM MASKS	1-2	± 0.25-0.5	10-30	450,000-500,000
X-RAY, CONTACT/ PROXIMITY	0.5-2	± 0.1-0.25	10-60	150,000-200,000
SCANNING ELECTRON BEAM, DIRECT-WRITE-ON WAFER	0.2-1	± 0.05-0.1	1-2* (COMMERCIAL MACHINES) UP TO 22-30* (IN-HOUSE)	1,000,000-2,000,000
*A function of resist, line width, wafer size, machine, etc.				

FIGURE H-1. Exposure Equipment Characteristics

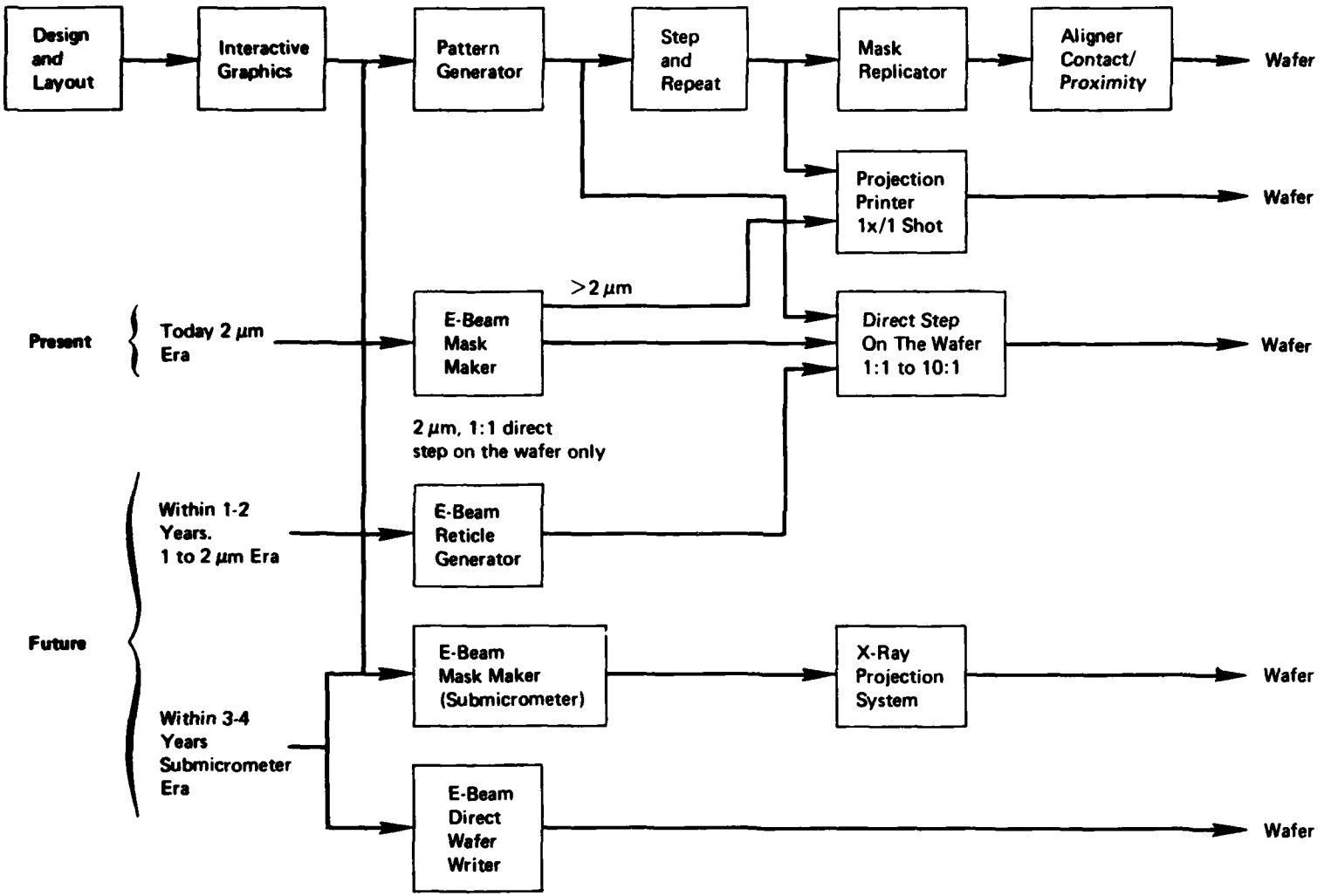

Figure H-2. Semiconductor Process Sequences described in terms of exposure method.

2. It is well known that the effective electron mobility in thin epiaxially-grown silicon films is a small fraction of the theoretical limit. Increasing this effective mobility in MOS devices could benefit VHSICs greatly. The research and equipment development required to make significant advances in circuit speeds is expensive, and it may not be done in time to benefit the VHSIC program without some funding.

3. The equipment used to make the metal interconnects on today's devices will not be adequate for sub-micron devices. Significant improvements in metal characteristics, step coverage, and other parameters must be made.

4. Much has been said about the requirements for improved methods of annealing. The methods and equipment used for today's devices will not be adequate for VHSICs. Some limited progress has been made using lasers and other sources for localized heating, but a good bit more progress is needed to meet the requirements of the VHSIC program.

5. Equipment for improved packaging for military use needs some development effort.

6. Testing is perhaps the most critical area of all, and the cost of progress is very high.

7. Improved automation is a necessity to control the processes and maintain the cleanliness required to make sub-micron devices effectively.

There are other areas that need development work in order to have the proper processing equipment available for the fabrication and testing of VHSICs but perhaps these are most critical.

Considering the basic questions about the impact of the VHSIC program on the equipment industry:

1. If the program is administered properly, and funding is provided to the semiconductor manufacturing equipment companies, the industry could benefit enormously. But even more importantly, DoD and the semiconductor industry can benefit even more because the processing and testing equipment will be available when it is needed. Perhaps the most significant factor to consider is that this equipment will be available from companies who will be capable and willing to support the equipment with parts, after-sales service, and a continuation of equipment upgrades as further progress is made.

2. If the VHSIC funding is provided to the device and DoD system suppliers, without provisions for getting the funding to the semiconductor process equipment suppliers, the impact will be negative. And, more importantly, the DoD will get far less for the money expended than they would otherwise get.

It is clear that several of the major gating processes require some significant equipment development, and those processes will not be available on any type of production basis until that equipment development is completed.

If the equipment is developed by companies whose business it is to sell and service that equipment, it will be available to all contractors and, furthermore, there will be a natural continuation and perpetuation of the good effects of the program--not only for the DoD but for all of the industry involved in the process.

Most of the process equipment suppliers are relatively small companies. Most have never had government contracts and are not capable of responding with the normal proposals required to meet the needs of government evaluation experts. However, these companies are very efficient and also very dynamic. They can get a good bit more done on a small budget than normal government contractors.

These companies will require funding assistance to meet the market needs of the 1980s. They will get that funding, either from the U.S. government or other U.S. sources, or they will get it from sources in Europe or Japan. There are large pockets of foreign funding available these days. There is no doubt whatever that the governments of Japan, Germany, France, and others have recognized the importance of the U.S. semiconductor manufacturing equipment industry. There are moves and offers being made almost daily. Now, what does it mean to the U.S. defense effort as well as the U.S. semiconductor industry if the process equipment suppliers are forced to turn to foreign sources for their capital? While the answer is uncertain, the long-range impacts cannot be favorable.


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